ABSTRACT OF THE DISCLOSURE

A chip scale package (CSP) comprises a flip chip and chip carrier with features to enhance its electrical and thermal performance. The flip chip connects to the chip carrier through alternating signal and ground connections. Top layer routing on the chip carrier substantially maintains ground-based guard isolation between neighboring signal lines. The arrangement of inter-layer vias and bottom layer traces also maintains the isolation for flip chip signals routed to the bottom layer of the chip carrier, where they are available for interconnection with a primary circuit board via solder balls or the like. The bottom layer further includes a centralized ground plane. Special thermal vias extend from the top layer into this bottom layer ground plane. Dedicated solder ball connections for the ground plane provide a ground path between the flip chip and the primary circuit with very low electrical and thermal impedances.